## ABSTRACT OF THE DISCLOSURE

A test circuit comprises a selector SEL1 having a first input to which signals M1OUT from a macro block MB1 are input and a second input to which test input signals TIN1 and TIN2 for a macro block MB2 are input, and a selector SEL2 having a first input to which a signal SQ from the SEL1 is input and a second input to which a signal M2OUT from the MB2 is input. In a first test mode in which the MB1 is tested, the SEL1 outputs the signals M1OUT from the MB1 to a first input of the SEL2, and the SEL2 outputs the signal SQ from the SEL1 to the MB1. In a second test mode in which the MB2 is tested, the SEL1 outputs the test input signals TIN1 and TIN2 for the MB2 to the MB2, and the SEL2 outputs the signals M2OUT from the MB2 as a test output signal TOUT for the MB2.